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10/709,022	04/07/2004	Yuan-Kun Hsiao	VOSP0004USA	3021

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EXAMINER
SINGH, HIRDEPAL

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/709,022	HSIAO, YUAN-KUN	
	Examiner	Art Unit	
	Hirdepal Singh	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the filing date of April 07, 2004. Claims 1-20 are pending and have been considered below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US 6,754,147) in view of Takumai et al. (US 2003/0081516) further in view of Von Kaenel (US 2003/0067335).

Regarding claim 1:

Hsu et al discloses a phase adjusting circuit (figure 6) for generating a phase adjusting value based on the phase difference of a target clock signal and an input signal, the phase adjusting circuit comprising:

a phase-frequency detector (12 in figure 6) for generating a first control signal and a second control signal by comparing the phase of the input signal with the phase of the target clock signal;

a decision logic circuit (104 and 106 in figure 6) connected to the counter for generating a third counting value based on the first counting value and the second counting value, calculating the sum of a plurality of the third counting values and comparing the sum with a predetermined range for outputting the phase adjusting value as the counting times are increased to equal to a predetermined (as clearly stated in claim 1 last limitation) counting times.

Hsu et al discloses all of the subject matter as described above except for specifically teaching (1) a clock generator for generating a reference clock; (2) a counter connected to the phase-frequency detector and the counter for generating a first counting value by counting the number of cycles of the reference clock during the duration of the first control signal, and generating a second counting value by counting the number of cycles of the reference clock during the duration of the second control signal.

However, regarding item (1) above, Takumai et al in the same field of endeavor discloses a system for adjusting the phase of the clock comprising a clock generator (system clock; paragraph 0075) for generating a reference clock; and regarding item (2) above, a counter (271 in figures 1 and 15) connected to the phase-frequency detector (270 which is further connected to 243 in figure 15).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine a counter between the phase frequency detector and control logic to count the number of pulses of the system clock signal as suggested by Takumai in Hsu system in order to get the information related to the phase difference of

the incoming signal and the target clock signal so that the counter starts counting based on the control signal i.e. whether the input signal leads or lags the target clock signal, in this way the target clock is easily adjusted and controlled according to the input signal also whenever there is a phase difference between input and target clock the phase adjustment circuit makes the adjustment quickly.

Also, regarding item (2) above, Von Kaenel in the same field of endeavor discloses a system for adjusting the phase of incoming clock signal where a counter (14 in figure 1) connected to the phase-frequency detector (12 in figure 1) and the counter for generating a first counting value by counting the number of cycles of the reference clock during the duration of the first control signal, and generating a second counting value by counting the number of cycles of the reference clock during the duration of the second control signal.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine a counter as used in Von Kaenel to count the number of pulses of the clock signal in Hsu system in order to get the information related to the phase difference of the incoming signal and the target clock signal so that the counter starts counting based on the control signal i.e. whether the input signal leads or lags the target clock signal, in this way the target clock is easily adjusted and controlled according to the input signal also whenever there is a phase difference between input and target clock the phase adjustment circuit makes the adjustment quickly.

Regarding claims 2 and 3:

Hsu et al discloses all of the subject matter as described above except for specifically teaching the first control signal is generated when the phase of the input signal leads the phase of the target clock signal and the second control signal is generated when the phase of the input signal lags the phase of the target clock signal.

However, Von Kaenel in the same field of endeavor discloses a system for adjusting the phase of the clock where the first control signal is generated when the phase of the input signal leads the phase of the target clock signal (paragraph 0018, lines 12-14) the second control signal is generated when the phase of the input signal lags the phase of the target clock signal (paragraph 0018, lines 14-16). Also Takumai et al in the same field of endeavor discloses the first control signal is generated when the phase of the input signal leads the phase of the target clock signal (paragraph 0071).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a counter in Hsu system in order to get the information related to the phase difference of the incoming signal and the target clock signal so that the counter starts counting based on the control signal i.e. whether the input signal leads or lags the target clock signal, in this way the target clock is easily adjusted and controlled according to the input signal also whenever there is a phase difference between input and target clock the phase adjustment circuit makes the adjustment quickly.

Regarding claim 4:

Hsu et al discloses all of the subject matter as described above except for specifically teaching that the predetermined range ranges from a positive number of a

half of the predetermined counting times to a negative number having an absolute value of a half of the predetermined counting times.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to set the predetermined range which goes from half of the predetermined count to negative number having an absolute value equal to half of the predetermined number because when the counter counts the two values for the leading or lagging phase of the incoming signal to the clock signal i.e. the two values are up/down or positive/negative values, so to generate the adjusting values it is required to see if the counter exceed a predetermined range i.e. the combined count (from negative value to positive value) is more than predetermined value in order to generate a delay signal to adjust the clock signal.

Regarding claim 5:

Hsu et al discloses all of the subject matter as described above except for specifically teaching that the first counting value is a positive value, the second counting value is a negative value, and the third counting value is the sum of the first counting value and the second counting value.

However, Takumai et al in the same field of endeavor discloses a system for adjusting the phase of the clock signal where a counter (271 in figures 1 and 15) counts a first positive counting value (paragraph 0075; figure 6).

Also Von Kaenel in the same field of endeavor discloses a system for adjusting clock signal where counter (14 in figure 1) counts a first positive counting value, the

second counting value is a negative value (paragraphs 0017, 0025 and 0035; the up counting value is positive and down counting value is negative), and the third counting value is the sum of the first counting value and the second counting value.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to implement a counter as taught by Takumai to control the phase of the incoming signal by adjusting the gain to change the frequency division ratio to further compensate for the phase and using the up/down or positive negative values of the Von Kaenel counter to control the phase (generate a decision or third value based on the up/down or positive negative values of the counter) of the incoming signal in Hsu system to make quick adjustment to the clock signal.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US 6;754,147) in view of Takumai et al. (US 2003/0081516) further in view of Von Kaenel (US 2003/0067335) as applied to claim 1 above, and further in view of Fukuhara (US 2002/0027966).

Regarding claim 6:

Hsu et al discloses all of the subject matter as described above except for specifically teaching that the phase-frequency detector is further able to receive a protection signal to stop outputting the phase adjusting value for avoiding interference generated from an unstable input signal.

However, Fukuhara in the same field of endeavor discloses a system for adjusting the phase of the clock signal where a phase-frequency detector is further able to receive a protection signal (paragraphs 0008 and 0065) to stop outputting the phase adjusting value for avoiding interference generated from an unstable input signal.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a protection signal in the phase adjusting circuit in order to stop it for sending phase adjustment signal to avoid an error occurred in the incoming wobble signal by the signal processing done on the modulated part of the signal i.e. the address containing part of the wobble signal is modulated and it could give an error signal which if used to adjust the clock of the wobble signal could cause the wrongly adjusted clock as the phase adjustment is influenced by the error generated in the wobble signal, the protection signal is able to avoid generating the wrong clock and makes the circuit work properly.

5. Claims 7, 13, 14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US 6,754,147) in view of Takumai et al. (US 2003/0081516).

Regarding claims 7 and 14:

Hsu et al discloses a clock signal adjusting circuit comprising:

a phase adjusting circuit (108 in figure 6) for generating a phase adjusting value based on an input signal and a target clock signal; and

Hsu et al discloses all of the subject matter as described above except for specifically teaching that a frequency divider connected to the phase adjusting circuit for adjusting the target clock signal by dividing the frequency of a first reference clock based on the phase adjusting value.

However, Takumai et al in the same field of endeavor discloses a system for adjusting the phase of the clock signal where a frequency divider (242 in figures 1 and 15) connected to the phase adjusting circuit for adjusting the target clock signal by dividing the frequency of a first reference clock based on the phase adjusting value.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a frequency divider as suggested by Takumai in Hsu system in order to make the phase and frequency of the incoming clock signal in accordance with the adjustment value to make the system clock correct which is advantageous as the clock is adjusted according to the wobble signal and the frequency divider and the delay value in combination make sure the correct clock signal.

Regarding claims 13 and 20:

Hsu et al discloses all of the subject matter as described above and further discloses that the system is applicable in an optical disc drive (title) where the input signal being a wobble signal of an optical disc, the target clock signal being a corresponding wobble clock (figure 6) generated by the optical disc drive based on the wobble signal.

6. Claims 8-11 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US 6,754,147) in view of Takumai et al. (US 2003/0081516) as applied to claims 7 and 14 above, and in view of Von Kaenel (US 2003/0067335) further in view of Fukuhara (US 2002/0027966).

Regarding claims 8 and 15:

Hsu et al discloses all of the subject matter as described above and further discloses:

a phase-frequency detector (12 in figure 6) for generating a first control signal and a second control signal by comparing the phase of the input signal with the phase of the target clock signal;

a decision logic circuit (104 and 106 in figure 6) connected to the counter for generating a third counting value based on the first counting value and the second counting value, calculating the sum of a plurality of the third counting values and comparing the sum with a predetermined range for outputting the phase adjusting value as the counting times are increased to equal to a predetermined (as clearly stated in claim 1 last limitation) counting times.

Hsu et al discloses all of the subject matter as described above except for specifically teaching (1) a clock generator for generating a reference clock; (2) a counter connected to the phase-frequency detector and the counter for generating a first counting value by counting the number of cycles of the reference clock during the duration of the first control signal, and generating a second counting value by counting

the number of cycles of the reference clock during the duration of the second control signal.

However, regarding item (1) above, Takumai et al in the same field of endeavor discloses a system for adjusting the phase of the clock comprising a clock generator (system clock; paragraph 0075) for generating a reference clock; and regarding item (2) above, a counter (271 in figures 1 and 15) connected to the phase-frequency detector (270 which is further connected to 243 in figure 15).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine a counter between the phase frequency detector and control logic to count the number of pulses of the system clock signal as suggested by Takumai in Hsu system in order to get the information related to the phase difference of the incoming signal and the target clock signal so that the counter starts counting based on the control signal i.e. whether the input signal leads or lags the target clock signal, in this way the target clock is easily adjusted and controlled according to the input signal also whenever there is a phase difference between input and target clock the phase adjustment circuit makes the adjustment quickly.

Also, regarding item (2) above, Von Kaenel in the same field of endeavor discloses a system for adjusting the phase of incoming clock signal where a counter (14 in figure 1) connected to the phase-frequency detector (12 in figure 1) and the counter for generating a first counting value by counting the number of cycles of the reference clock during the duration of the first control signal, and generating a second counting

value by counting the number of cycles of the reference clock during the duration of the second control signal.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine a counter as used in Von Kaenel to count the number of pulses of the clock signal in Hsu system in order to get the information related to the phase difference of the incoming signal and the target clock signal so that the counter starts counting based on the control signal i.e. whether the input signal leads or lags the target clock signal, in this way the target clock is easily adjusted and controlled according to the input signal also whenever there is a phase difference between input and target clock the phase adjustment circuit makes the adjustment quickly.

Regarding claims 9, 10, 16 and 17:

Hsu et al discloses all of the subject matter as described above except for specifically teaching the first control signal is generated when the phase of the input signal leads the phase of the target clock signal and the second control signal is generated when the phase of the input signal lags the phase of the target clock signal.

However, Von Kaenel in the same field of endeavor discloses a system for adjusting the phase of the clock where the first control signal is generated when the phase of the input signal leads the phase of the target clock signal (paragraph 0018, lines 12-14) the second control signal is generated when the phase of the input signal lags the phase of the target clock signal (paragraph 0018, lines 14-16). Also Takumai et

al in the same field of endeavor discloses the first control signal is generated when the phase of the input signal leads the phase of the target clock signal (paragraph 0071).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a counter in Hsu system in order to get the information related to the phase difference of the incoming signal and the target clock signal so that the counter starts counting based on the control signal i.e. whether the input signal leads or lags the target clock signal, in this way the target clock is easily adjusted and controlled according to the input signal also whenever there is a phase difference between input and target clock the phase adjustment circuit makes the adjustment quickly.

Regarding claims 11 and 18:

Hsu et al discloses all of the subject matter as described above except for specifically teaching that the predetermined range ranges from a positive number of a half of the predetermined counting times to a negative number having an absolute value of a half of the predetermined counting times.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to set the predetermined range which goes from half of the predetermined count to negative number having an absolute value equal to half of the predetermined number because when the counter counts the two values for the leading or lagging phase of the incoming signal to the clock signal i.e. the two values are up/down or positive/negative values, so to generate the adjusting values it is required to see if the counter exceed a predetermined range i.e. the combined count (from negative

value to positive value) is more than predetermined value in order to generate a delay signal to adjust the clock signal.

7. Claims 12 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US 6,754,147) in view of Takumai et al. (US 2003/0081516) as applied to claims 7 and 14 above, and further in view of Nakao et al. (US 5,939,947).

Regarding claims 12 and 19:

Hsu et al discloses all of the subject matter as described above except for specifically teaching that the frequency divider comprises:

a counter for counting the cycle number of cycles of the first reference clock and resetting the cycle number after each predetermined number of cycles of the first reference clock; a register for storing the phase adjusting value; a comparator connected to the counter and the register for generating an enable signal when the cycle number of the first reference clock is equal to the phase adjusting value; a pulse generator connected to the comparator for generating an impulse when receiving the enable signal; a flip-flop having a trigger input terminal connected to the pulse generator for outputting the target clock signal while receiving the impulse; and an inverter having an input terminal for receiving the target clock signal and inverting the target clock signal to feedback to the input of the flip-flop.

However, Nakao et al in the same field of endeavor discloses that the frequency divider comprises a counter (38b in figures 1 and 3) for counting the cycle number of

cycles of the first reference clock and resetting the cycle number after each predetermined number of cycles of the first reference clock; a register (40 in figures 1 and 3) for storing the phase adjusting value; a comparator (3b in figures 1 and 3) connected to the counter and the register for generating an enable signal when the cycle number of the first reference clock is equal to the phase adjusting value; a pulse generator connected to the comparator for generating an impulse when receiving the enable signal (column 3 lines 60-66); a flip-flop (39 in figures 1 and 3) having a trigger input terminal connected to the pulse generator for outputting the target clock signal while receiving the impulse; and an inverter having an input terminal for receiving the target clock signal and inverting the target clock signal to feedback to the input of the flip-flop (column 4, lines 1-10).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a frequency dividing circuit comprising a counter, register, comparator, pulse generation means, flip flop and feeding back the inverted output of flip flop as the advantage of using a frequency dividing circuit comprising these components is to get the clock signal which is true wobble clock signal.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hirdepal Singh whose telephone number is 571-270-

1688. The examiner can normally be reached on Mon-Fri (Alternate Friday Off)8:00AM-5:00PMEST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HS
August 29, 2007

SHUWANG LIU
SUPERVISORY PATENT EXAMINER

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :10/25/05, 11/08/05, 8/29/06, 9/05/06, 9/12/06, 4/16/06, 6/19/07.